(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 1 134 799 A1

(12) EUROPEAN PATENT APPLICATION

(43) Date of publication:
19.09.2001 Bulletin 2001/38

(51) Int Cl.[7]: **H01L 21/336**, H01L 21/28

(21) Application number: **00830197.0**

(22) Date of filing: **15.03.2000**

(84) Designated Contracting States:
AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE
Designated Extension States:
AL LT LV MK RO SI

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(54) Reduced thermal process for forming a nanocrystalline silicon layer within a thin oxide layer

(57) A process for forming a thin layer of Silicon nanocrystals in an oxide layer is disclosed. The process comprises, on a semiconductive substrate, thermally oxidizing a first portion of the substrate into an oxide layer, forming Silicon ions within the layer of oxide, and thermally treating the Silicon ions to become the thin layer of Silicon nanocrystals. In the inventive process the formation of the Silicon ions is by ionic implantation of the Silicon ions into the oxide at an ionization energy of between .1 keV and 7keV, and preferably between 1 and 5 keV. This allows the Silicon atoms to coalesce in a lower temperature than would otherwise be possible. Additionally, more than one layer of nanocrystals can be formed by performing more than one implantation at more than one energy level. Embodiments of the invention can be used to form non-volatile memory devices with a very high quality having a very small size.

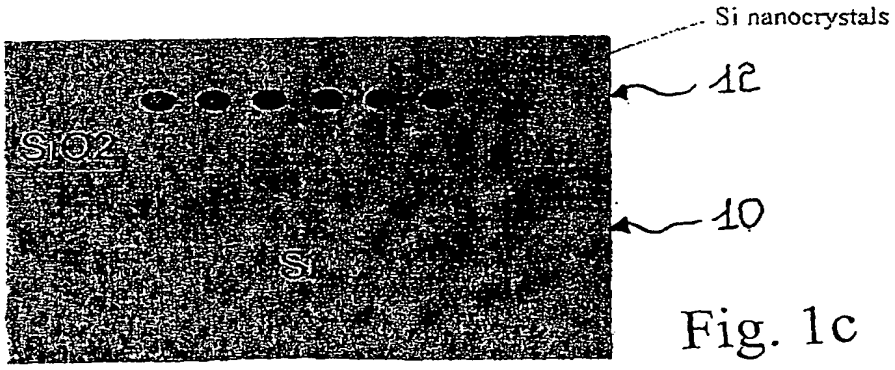

Fig. 1c

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Description

Field of the application

[0001] The present invention is directed toward forming a nanocrystalline silicon layer within a thin oxide layer, and to a process for forming the nanocrystalline silicon layer using a lower processing temperature than those processes used previously.

[0002] More specifically, the present invention is directed toward a process for forming an oxide layer containing a continuous polysilicon layer comprising forming the oxide layer on a semiconductive substrate, introducing Silicon ions within the oxide layer, and thermally treating the semiconductive substrate to cause the Silicon ions to become the continuous polysilicon layer.

Prior Art

[0003] Advanced electronics and opto-electronic devices can be fabricated using the carrier confinement and Coulomb blockage effects of a layer of nanometer-sized Silicon crystals, commonly referred to as Si quantum dots.

[0004] References in the area of Si quantum dots include *Nanotechnology*, Gregory Timp, Editor, Springer-Verlag, New York (1999) (and references contained within); as well as *A Silicon nanocrystals Based Memory, S.* Tiwari et al., Appl. Phys. Lett. 68, 1377 (1996); *The Integration of Nanoscale Porous Silicon Light Emitters: Materials Science, Properties and Integration with Electronic Circuitry,* P.M. Fauchet, Journal of Luminescence 80, 53 (1999); and *Room-Temperature Single-Electron Memory,* K. Yano et al., IEEE Trans. on Electronic Devices ED-41, 1628 (1994).

[0005] One area of electronics using Si quantum dots to a great success is the formation of non-volatile memory devices. In such devices, a layer of Si quantum dots within a thin dielectric' layer, such as a gate oxide, is used in place of the more typical structure of an entire polysilicon layer (floating gate) formed within a thicker oxide.

[0006] Examples of non-volatile memories formed by nanocrystalline silicon include US Patents 5,852,306 and 5,959,896, both by Leonard Forbes and both assigned to Micron Technology, Inc.

[0007] Additionally, light emitting Silicon devices are being produced with a layer of Si nanocrystals that are embedded within a Silicon Dioxide layer.

[0008] Forming the Si nanocrystals can be achieved by a variety of techniques, such as plasma-enhanced vapor deposition, aerosol techniques, or Si implantation, for example.

[0009] Several strict requirements must be met for a successful use of Si quantum dots in most applications.

[0010] First, it is necessary that a localized layer of small (1-3 nanometer in diameter) Si nanocrystals that have a very uniform size distribution be formed within a very thin (10-40 nm) layer of Silicon Dioxide (SiO_2) that has excellent electronic properties. Second, the density of defect states at the interface between the Si nanocrystals and the SiO_2 must be minimal. Finally, the thermal temperature of the processing or annealing step should be as low as possible.

[0011] This last requirement, that of a low processing temperature can be crucial in many applications. In particular, for this application, the nanocrystal array should be formed with a thermal process at temperatures below 1000° C. High temperatures are not compatible with the fabrication flow-chart of advanced devices. These high temperatures are therefore to be avoided, to the extent possible.

[0012] Until now, the only method by which this goal can be achieved is by depositing amorphous Silicon and crystallising it into polysilicon at 750° C, as disclosed in the *K. Yano et al.* article cited above.

[0013] However, this method results in the formation of a discontinuous polysilicon layer, and the thickness variations in the film makes reproducibility and control of the process quite critical.

[0014] On the other hand, alternative methods using Silicon rich oxide layers that are produced by deposition of a substechiometric oxide layer, require a thermal process at a temperature above 1050°C in order to form the Si nanocrystals through the agglomeration of the excess Silicon.

[0015] Thus, in the prior art there is no controlled process whereby the necessary processes can be performed in a low thermal environment.

[0016] The technical problem at the basis of the present invention is that of finding a method for implanting Silicon ions into a thin oxide layer such that a subsequent thermal processing step can be performed within a low thermal budget. Additionally, the method must provide that the Silicon ions are implanted at a precise depth, such that no over lateral or horizontal dispersion occurs. The method must have such characteristics that overcomes the limitations and/or the drawbacks which, at the moment limit the methods for implanting Silicon ions into a thin oxide according to the prior art.

Summary of the Invention

[0017] The resolutive idea at the basis of the present invention is that of implanting into a thin oxide layer, Silicon ions by ion implantation at a low energy, such that annealing needed for the formation of the nanocrystal can be performed at a low thermal budget. Additionally, Silicon ions implanted at such a low energy level have low incidence of horizontal or lateral dispersion.

[0018] The present invention uses an ultra-low energy Silicon ion implantation that successfully introduces Si ions in an oxide layer to produce a localized layer of Si nanocrystals in a process that is easily integrated with existing semiconductor fabrication processes.

[0019] On the basis of such idea for a solution the technical problem is resolved by a method of the type previously indicated and defined by claim 1.

[0020] The characteristics and advantages of the device according to the invention will be seen from the description, following herein, of an embodiment given as an indication and not limiting with reference to the drawings attached.

Brief Description of the Drawings

[0021] Figures 1a, 1b and 1c are cross-sectional views of a silicon wafer showing steps in the inventive process, according to an embodiment of the invention.

[0022] Figures 2a and 2b are electron microscopy photographs showing results of Silicon ions implanted in a Silicon Dioxide layer.

[0023] Figure 3 is a cross sectional view of a floating gate memory cell formed by the process described with reference to figures 1a, 1b, and 1c.

Detailed Description

[0024] A repeatable process that creates uniform, small-sized and high density Si quantum dots in thin oxides or other tunnelling oxides is disclosed.

[0025] With reference to Figures 1a, 1b and 1c, the example used to describe the inventive process is that of forming Si quantum dots in a thermally grown SiO_2 gate oxide. It is clear, however, to those skilled in the art that this method can be used for the formation of dots with other materials (such as for example Ge, Sn, Au, etc.) into various dielectric films (oxides, nitrides, etc.) either grown or deposited on semiconductor materials. Discussion of structures or processes well known to those skilled in the art has been abbreviated or eliminated for brevity.

[0026] The process steps and structures described below do not form a complete process flow for manufacturing integrated circuits. The present invention can be practiced in conjunction with integrated circuit fabrication techniques currently used in the art, and only so much of the commonly practices process steps are included as are necessary for an understanding of the present invention. The figures representing cross-sections of portions of an integrated circuit during fabrication are not drawn to scale, but instead are drawn so as to illustrate the important features of the invention.

[0027] The use of ion implantation at traditional energies (*i.e.*, higher than 20 keV) for the synthesis of localized arrays of Si nanocrystals presents two major problems.

[0028] First, the implanted ions are largely dispersed, about 14 nm for a 20 keV Si implant, which produces a broad depth *(i.e.,* vertical) distribution of the excess Si. This results in a broad depth distribution of the nanocrystals formed when the Si quantum dots are thermally treated.

[0029] Second, because the diameter of a Si quantum dot can only grow by accumulating excess Si atoms in a volume of radius $\sqrt{Dt}$around the nucleus (where D is the diffusion coefficient of Silicon at the annealing temperature, and where t is the annealing time), crystallization will only take place when the temperature is above a critical value. In the prior art solutions, implanting the Silicon ions at the high energy implant causes a large spatial distribution of ions, *i.e.*, they are not very close to one another after implantation. Because D is very small (*i.e.*, approx. $10^{-16}/cm^2$ even at 1100°C) and because in these prior art solutions the distance between implanted Silicon ions is relatively large, temperatures above 1000°C are needed in order to form nanocrystals with 1-3 nm size. Therefore, this high thermal process can only be used in semiconductor fabrications where exposure to a high temperature will not damage the circuitry being formed.

[0030] Third, the broad distribution of the excess Silicon ions results in both broad lateral and depth distribution of the nanocrystals formed after the thermal process.

[0031] These above problems prevent prior art circuits from performing at the optimum levels possible. On the contrary, in the present invention, the use of extremely low energy (< 5 keV) Si ion implantation results in an extremely narrow as implanted ion concentration profile. For example, a 1 keV Si ion implanted into SiO_2 has a projected depth range of only approx. 5 nm and a lateral dispersion of only 1.5 nm.

[0032] Furthermore, due to the reduced dispersion, extremely high peak Si concentration is achieved. For example, a peak concentration of $5 \times 10^{22}/cm3$, corresponding to the atomic density of bulk Silicon, is achieved by a 1KeV Si implant to a fluence (*i.e.*, the number of implanted atoms per square area of silicon) of $2 \times 10^{16}/cm2$.

[0033] In these conditions, the growth and hence the crystallization of the agglomerates are dominated by the coalescence of the high density of smaller Si aggregates found at the ion end of the range, rather than being limited by the long range diffusion of the Silicon ions.

[0034] This produces a considerable reduction in the required thermal budget, or the overall time and temperature of the finishing steps that require heat treatment. In particular, the inventors have found that nanograins (small portions of agglomed Silicon) are already formed in temperatures as low as 700°C.

[0035] This low energy implantation forms a buried polysilicon layer within the oxide layer.

[0036] With reference to figure la, shown is a Silicon semiconductor substrate 10, on which a Silicon Dioxide layer 12 has been grown. In a standard masking step, a layer of energy-sensitive material, such as a photoresistive layer is deposited on the Silicon Dioxide layer 12. After partially covering, exposing and developing this photoresistive layer, remaining on the Silicon Dioxide layer 12 is a implantation block 14, a portion of which is

shown in Figure Ia, and an opening 16 is formed in the implantation block. Low energy Silicon ions are implanted at an energy between .1keV and 10keV, with energy levels between 1keV and 5keV being preferred. At this energy, the Silicon ions are driven into the Silicon Dioxide layer 12 at a very specific location, between a top surface 18 and the junction of the substrate 10 with the Silicon Dioxide layer 12. Controlling the implantation energy determines where the Silicon ions will be placed in the Silicon Dioxide layer 12. Also, at these low implantation energies, the Silicon ions are very localized, and do not disperse much in either a horizontal or vertical direction. In other words, the Silicon ions, after being implanted by the low implantation energy, are closely grouped.

[0037] Figure 1b shows an embodiment of the invention where a buried polysilicon layer 20 is formed within the Silicon Dioxide layer 12. After the Silicon ions have been implanted into the Silicon Dioxide layer 12, the structure is heated at a low temperature, for instance 700 - 800°C, causing excess Silicon ions to fuse into the buried polysilicon layer 20.

[0038] Figure 1c shows an embodiment of the invention where a nanocrystal array 22 is formed within the Silicon Dioxide layer 12. In this embodiment, after the Silicon ions have been implanted, the structure is heated to a low temperature, for instance 700 - 800°C, in the presence of an oxidizing agent such as an ambient atmosphere containing N_2 and O_2. Again the vertical and lateral dispersion of the Silicon ions is very low when the Silicon ions are implanted at low energy levels. The heating of the structure causes the Silicon ions to group together in clusters, thereby forming an array of nanocrystals 22 at the desired location within the Silicon Dioxide layer 12.

[0039] Figure 2a is a scanning electron microscope photograph that shows the actual results of Si quantum dots implanted into a Silicon Dioxide layer that is 25nm thick. In this embodiment the Silicon ions were implanted at an energy of 5 keV and a fluence of 5×10^{16}/cm2 into the Silicon Dioxide layer. After thermal treatment, the resultant continuous polysilicon layer is 5 nm thick.

[0040] Figure 2b shows the actual results of Si quantum dots implanted into a Silicon Dioxide layer that is 15 nm thick. In this embodiment, the Silicon ions were implanted at an implantation energy of 1 keV and a fluence of 2×10^{16}/cm2. Subsequent thermal treatment with oxidation produces a dense array of small (1.5nm in diameter) Si nanocrystals having a very localized position.

[0041] The depth of the buried Silicon layer is determined by the projected range of the ions (which can be changed from 2 nm for implants at 0.2 keV to 10 nm for implants at 5 keV. Note that the polysilicon layer is fully confined within the SiO2 layer even for an extremely thin layer of oxide. No interaction of the excess Silicon with either surface or Si/SiO2 interface has been observed.

[0042] The grain size in the layer, and hence the maximum dimension of the Si nanocrystals in the polysilicon layer is determined by the lateral diffusion of the ion distribution which can be as small as 3nm for a 1 keV implant.

[0043] These continuous polysilicon layers can be transformed into well localized arrays of Silicon nanocrystals by performing a low temperature (e.g. 800°C for 1 hour) oxidation in a $N_2 + O_2$ ambient atmosphere. The process results in a preferential oxidation along the grain boundary, and hence in the separation of the various grain. The final array consists of well localized nanocrystals with a sharp grain size distribution.

[0044] Figure 3 shows an example of a non-volatile memory cell 70 produced using one of the inventive processes. In a Silicon semiconductor substrate 50, a source 52 and a drain 54 are conventionally produced. A thin Silicon Dioxide layer 56 is grown on the semiconductor substrate 50. A mask is formed on the Silicon Dioxide layer 56 and an opening produced within the mask (mask and opening not shown). The opening roughly approximates the distance between the source 52 and the drain 54 in this example. Silicon ions are implanted into the Silicon Dioxide layer 56 and then thermally treated in an oxidizing environment to produce an array of nanocrystals 60. The size and depth of the nanocrystal array will depending on the energy of implantation and the number of Silicon ions implanted.

[0045] After the nanocrystal array has been established, a Polysilicon gate layer 62 is formed on the Silicon Dioxide layer 56. Of course, the source 52 and the drain 54 can be formed before or after the growing of the Silicon Dioxide layer 56, or even after the formation of the Polysilicon gate layer 62.

[0046] Many advantages are afforded by embodiments of this invention in comparison with the prior art techniques.

[0047] Low energy ion implantation is an extremely reliable process able to be used in the advanced formation of semiconductor circuits with little modification of existing processes.

[0048] The low energy ion implantation is a clean process, and does not introduce any contaminates such as Nitrogen and Hydrogen which are found when a plasma-assisted process is used. Presence of these contaminates degrades device performance.

[0049] Nanocrystals that are fully embedded in a thermally grown oxide can be formed, thus achieving a perfect interface between the nanocrystals and the SiO_2 matrix. This cannot be achieved by the other prior art methods since the thermal treatments of non-stechiometric oxides results in Si nanocrystals embedded in a SiO_x matrix. Non-stechiometric oxides are used in plasma-enhanced chemical vapor deposition, and in other methods.

[0050] The dimensions of the nanocrystals can be carefully controlled by lateral ion diffusion which is extremely low at energies below 1keV. This ensures that the Si nanocrystals having diameters as small as 1 to 2 nm can be regularly formed.

[0051] Using a thermal process following ion implantation can guarantee a process dominated by the nucleation rather than diffusion-mediated growth. Hence, the energy and diffusion of the implant can be used to fix the location of the array of Si quantum dots and the average dimension of the dots.

[0052] The process is easily assimilated into the current state of the art production techniques. For example, it can be patterned by using implants through a mask, thus solving the problems encountered in the etching of thin Silicon-rich films.

[0053] Either a continuous polysilicon layer or a distributed array of Silicon nanocrystals can be formed by properly changing the ion fluence. Additionally, more than one separate layer can be formed by performing multiple ion implantations having different energies.

[0054] The dimensions of the quantum dots can be controlled by only changing the ion fluence and the thermal treatments.

[0055] One non-limiting example of application is the fabrication of advanced non-volatile memories in which the continuous floating gate is replaced by an array of Si quantum dots. The potential innovation in this structure (which has been proposed by *K. Yano et al.*, and by *S. Tiwari et al.*, both cited above) in terms of operation voltage and programming times, can be fully explored only if a reliable technology for the fabrication of nanometer scale dots with high throughput and good uniformity in size and positions is available. Such technology is afforded by embodiments of the invention.

Claims

1. A process for forming an oxide layer (12) containing a continuous polysilicon layer (20) comprising: forming the oxide layer (12) on a semiconductive substrate (10), introducing Silicon ions within the oxide layer (12), and thermally treating the semiconductive substrate (10) to cause the Silicon ions to become the continuous polysilicon layer (20), **characterised in that** the introduction of Silicon ions within the oxide layer (12) is by ionic implantation of the Silicon ions into the oxide layer (12) at a low energy level under 20 keV.

2. The process of claim 1 wherein the oxide layer (12) is thermally grown to a thickness of between 10 and 40 nm prior to being implanted.

3. The process of claim 1 **characterized in that** the energy level of the ionic implantation is between . 1 and 7 keV.

4. A process for forming a distributed array of Silicon nanocrystals (22) a controlled distance from a first top surface (18) of a Silicon Dioxide layer (12) and a second controlled distance from a second bottom surface of the Silicon Dioxide layer, the process comprising: forming a Silicon Dioxide layer (12) on the Silicon substrate (10), forming a masking layer (14) disposed on the Silicon Dioxide layer (12), forming at least one opening (16) in the masking layer (14), implanting Silicon ions through the at least one opening (16) in the masking layer and into the Silicon Dioxide layer (12), and thermally treating the silicon substrate (10) to cause the Silicon to become the distributed array of Silicon nanocrystals (22), **characterized in that** implanting the Silicon ions is performed by ionic implantation at an ionization energy of between 1 keV and 7keV.

5. The process of claim 4 further **characterized in that** a lateral width of the Silicon nanocrystals (22) is controlled by controlling the lateral dispersion of the implanted Silicon ions.

6. The process of claim 4 **characterized in that** controlling the first controlled distance and the second controlled distance is performed by changing the ion implantation energy levels.

7. The process of claim 4 further **characterized in that** a second distributed array of Silicon nanocrystals (22) is formed by ionic implantation of further Silicon ions at another low ionization energy that is different than the ionization energy of the first implantation.

8. The process of claims 1-7 further **characterized in that** thermally treating the Silicon ions is performed at a temperature between 700 and 800°C.

9. A process for forming an oxide layer containing a layer of Silicon nanocrystals (22), comprising: forming the oxide layer on a semiconductor substrate (10), introducing Silicon ions into the oxide layer (12), and thermally treating the semiconductor substrate to cause the Silicon ions to form into the Silicon nanocrystals (22), **characterized in that** the introduction of the Silicon ions into the oxide (12) is by ionic implantation having a fluence of 2×10^{16}/cm2 at an ionization energy of approximately 1keV, and further **characterized in that** thermally treating the Silicon ions comprises transforming them into the Silicon nanocrystals (22) at a temperature of approximately 700°C.

10. A process for forming a non-volatile memory device (70) comprising: on a semiconductive substrate (50), thermally oxidizing a first portion of the substrate into a tunnel oxide (56), forming a masking layer on the tunnel oxide and forming an opening in the masking layer, depositing Silicon ions into the layer of tunnel oxide (56) through the opening in the masking layer, thermally treating the Silicon ions to

become a thin layer of Silicon nanocrystals (60), forming source (52) and drain (54) regions in the substrate (50), and forming a control gate (62) disposed over the tunnel oxide (56), **characterised in that** the deposition of the Silicon ions into the layer of tunnel oxide (56) is achieved through ionic implantation of the Silicon ions into the tunnel oxide (56) at an ionization energy of between 1 keV and 7keV.

11. The process of claim 10 further **characterized in that** the thermal treatment of the Silicon ions to become the thin layer of nanocrystals (60) is performed at a temperature between 700 and 800°C.

12. The process of claim 10 further **characterized in that** thermally oxidizing a first portion of the substrate (50) into the tunnel oxide (56) is performed in the presence of Nitrogen gas in order to produce a nitrided tunnel oxide (56).

13. The process of claims 1-11 further **characterized in that** the thermal treatment is performed in the presence of a high concentration of Nitrogen in order to increase the nucleation of the Silicon ions into Silicon agglomerates.

14. The process of claim 13 wherein the high concentration of Nitrogen reduces the annealing temperature necessary to cause agglomeration of the Silicon ions.

15. The process of claim 14 further **characterized in that** the thermal treatment of the Silicon ions is performed in a Nitrogen atmosphere.

16. The process of claims 1-15 further **characterized in that** the ionic implantation of the Silicon ions is preferably performed between 1 keV and 5keV.

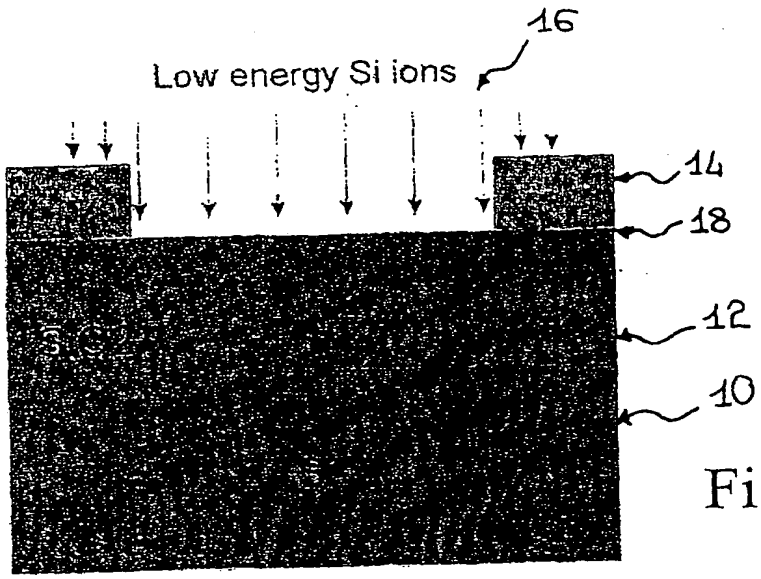

Fig. 1a

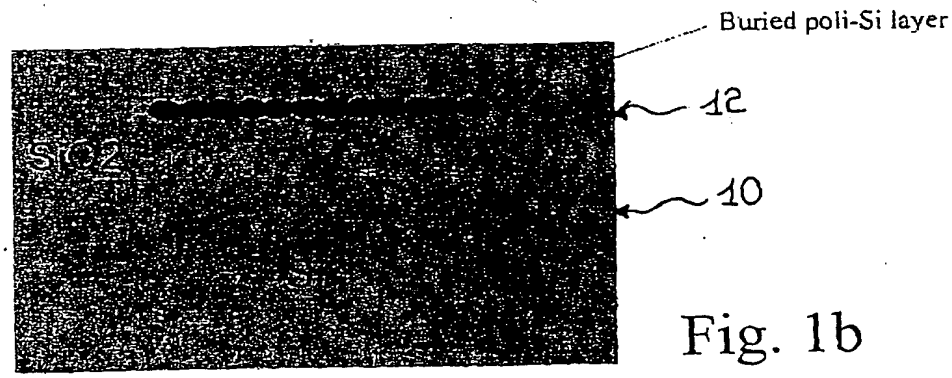

Fig. 1b

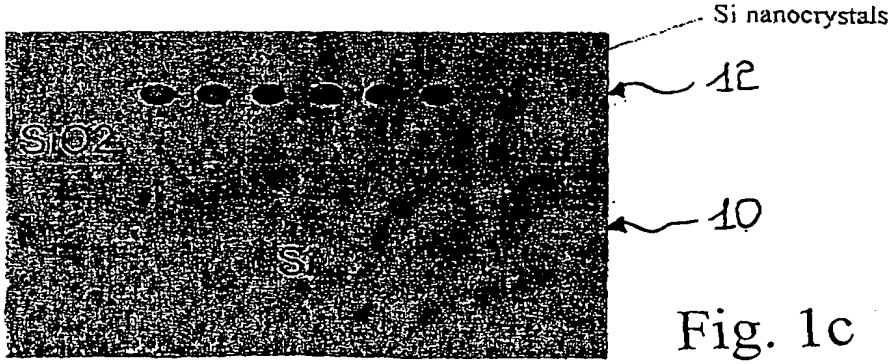

Fig. 1c

Fig. 2a

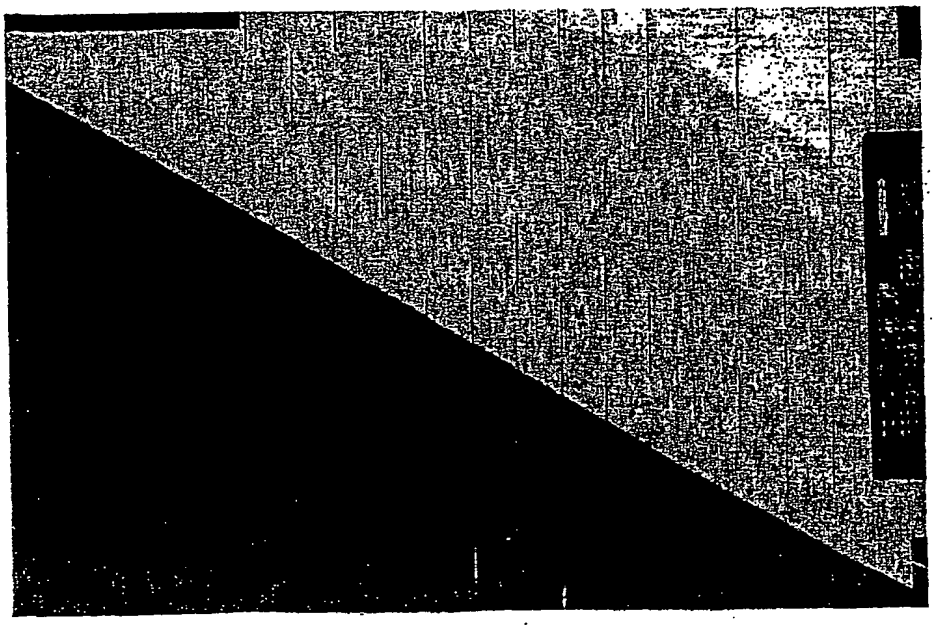

Fig. 2b

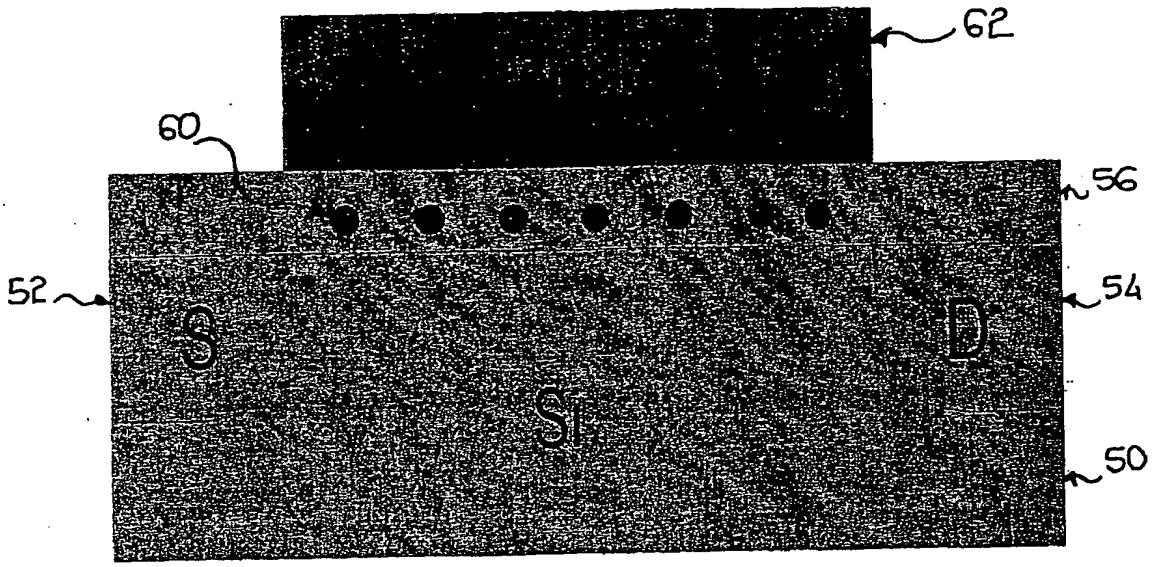

Fig. 3

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 00 83 0197

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The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
BERLIN	17 July 2000	Le Meur, M-A

CATEGORY OF CITED DOCUMENTS

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